Single-Crystal Semiconducting Chromium Disilicide Nanowires Synthesized via Chemical Vapor Transport

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Single-crystal $CrSi_2$ nanowires were synthesized for the first time by a chemical vapor transport (CVT) method, using $CrSi_2$ powder as the source material and iodine as the transport reagent. Structural characterization using electron microscopy, powder X-ray diffraction, and energy dispersive spectroscopy shows that these nanowires are hexagonal $CrSi_2$ single-crystal structures along the <001> growth axis, with diameters ranging from 20 to 300 nm and length up to 100 μm. Two-terminal electrical transport measurements show that these NWs have an estimated average resistivity of 4.4×10^{-3} Ω cm and behave like a degenerate semiconductor. These novel semiconducting silicide nanowires will be useful for optoelectronic and thermoelectric applications. The reported CVT method can be general for the chemical synthesis of other metal silicides.

Introduction

Transition-metal silicides, the family of refractory intermetallic compounds formed between metals and silicon, have diverse physical properties that are both very useful and fundamentally significant. Among them, semiconducting silicides[1] have been extensively investigated for optoelectronics[2] such as LEDs[3,4] and IR detectors[5] that are compatible with existing silicon CMOS microelectronics.[6] The narrow band gap semiconducting silicides, such as $CrSi_2$ and β-$FeSi_2$, have also been targeted and used (β-$FeSi_2$) for robust, stable, and inexpensive thermoelectric (TE) materials[1,7] and have shown promise for photovoltaic applications.[8] Specifically, chromium disilicide ($CrSi_2$) is an indirect narrow-gap (E_g = 0.35 eV) semiconductor[9−11] that has a Seebeck coefficient greater than 200 μV/K[9,12] and thermoelectric figure of merit (*ZT*) up to 0.25 at 900 K.[1,7] Although such a *ZT* value is modest compared with those of the more well-known TE materials,[7] refractory silicide materials would have the advantages of low cost, excellent thermal stability and mechanical strength, and outstanding oxidation resistance (protected by the self-limited surface oxidation of silicon), making them suitable for high-temperature applications.[1]

It has been predicted that reduced nanoscale dimension,[13,14] especially 1D quantum confinement,[13] of semiconductor materials will enhance the thermoelectric figures of merit (*ZT*) relative to their bulk values through increased density of states due to quantum confinement and enhanced surface phonon scattering. Guided by such theoretical predictions, an impressive demonstration of high *ZT* has been achieved using exquisitely engineered 2D superlattice nanostructures,[15] though contribution of the quantum confinement to thermoelectric properties has not yet been confirmed experimentally. Synthesis of 1D nanomaterials of those famous TE materials, such as Bi_2Te_3 using electrochemical deposition,[16] has been difficult and problematic.[17] Measurements on these soft, rough, mostly polycrystalline and defect-prone nanowires have not demonstrated conclusive improvement of TE properties. Making high-quality, single-crystal, mechanically robust, and controllably doped nanowires of thermoelectric semiconducting silicides would significantly enhance their *ZT*, thus having fundamental and practical importance. Moreover, it would be interesting to integrate high-quality nanowire building blocks of semiconducting $CrSi_2$ into nanophotonic devices.[18,19] Therefore, we are pursuing the rational chemical nanowire synthesis of this class of semiconducting silicides.

Even though there have been many examples of nanowire materials[20] of elemental semiconductors, oxides,[21] sulfides, and III−V compounds,[22] free-standing nanowires of silicides have only recently begun to emerge.[23−25] General and

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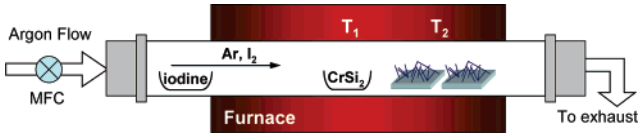

Figure 1. Schematic setup for the synthesis of $CrSi_2$ nanowires using chemical vapor transport (CVT).

rational synthesis of silicide nanowires is challenging partially because of the multiple stoichiometries and complex phase behavior of many silicide compounds,[26] which are markedly different from the simple prototypical semiconductors. Moreover, silicides usually have high melting points; for example, the mp of $CrSi_2$ is about 1460 °C. Unlike many oxide or sulfide NW syntheses, simply heating silicide solids is not very effective in delivering the materials in the vapor phase for synthesis of NWs with stoichoimetric control. To address these challenges, we have developed a chemical vapor deposition (CVD) approach using single-source organometallic precursors to synthesize silicide NWs such as FeSi and CoSi on silicon substrates covered with a thin (1−2 nm) layer of silicon oxide without any catalyst seeds.[24] We believe we have observed a new and unique NW growth mechanism that is different from the typical VLS NW growth[20,22,27] but generally applicable to silicide NW formation.

However, analogous organometallic compounds that appear suitable as the precursors for vapor-phase synthesis of $CrSi_2$ NWs are not readily available. Herein we develop a complementary method of chemical vapor transport (CVT) to deliver the gaseous precursors in the desired stoichiometry to enable the direct chemical synthesis of $CrSi_2$ NWs. CVT[28,29] is an established solid-state chemistry technique often used for growing single crystals. It relies on the reversible reactions of a transport reagent (often halogens) with a solid target material. The reaction occurs at one temperature (*T*1) that produces gas-phase products that subsequently undergo the reverse thermodynamic reaction at another temperature (*T*2) that deposits the target solid downstream (Figure 1). We will utilize the following CVT reaction[29,30] to deliver Cr and Si at a temperature of 900 °C, much lower than the mp (1460 °C) of $CrSi_2$

$$CrSi_2(s) + 5I_2(g) \leftrightarrow CrI_2(g) + 2SiI_4(g) \qquad (1)$$

Such stoichiometric delivery of precursors, in combination with the critical silicon oxide thickness control on silicon growth substrates,[31] allowed us to synthesize high-purity, single-crystal free-standing $CrSi_2$ nanowires in high yield for the first time. We also report the complete structural characterization and basic physical properties of the resulting semiconducting NWs. The reported chemical vapor transport methods will also be generally applicable for the vapor-phase synthesis of a wide range of nanowire[25] materials with complex phase behaviors and low vapor pressures.

Experimental Section

Growth Substrate Preparation. Silicon wafer chips roughly 1.2 cm by 2 cm in size were etched in a 5% HF solution for 10 min to remove the existing thermal or native silicon oxide layer, rinsed in deionized water, and dried in a stream of nitrogen gas. A thin 1−2 nm surface oxide layer was then regrown, using one of the following two methods. (i) A wet oxidation treatment: heating the substrates in stirred "metal etch" solution (30% H_2O_2: 37% HCl: H_2O = 1:1:5 v/v) at 70 °C for 10−20 min, followed by rinsing in deionized water and drying using N_2. (ii) UV oxidation method: irradiating the substrates under a 254 nm UV lamp (18 mW/cm^2) for 60 min. Following either oxidation method, a 2.0 μL aliquot of a 0.02 M solution of $Ni(NO_3)_2$ in ethanol was applied to each substrate using a micropipette and was allowed to dry in air before NW growth.

CVT Nanowire Growth Reactions. A home-built continuous-flow CVT reactor (Figure 1) was used, which is composed of a 22 mm diameter quartz tube heated by a Lindberg\Blue M tube furnace with 1 in. inner bore, a mass-flow controller (MFC), and liquid traps located downstream from the furnace to neutralize reaction products. $CrSi_2$ powder (ca. 100 mg, usually about 30 mg consumed) was placed in an alumina boat in the center of the furnace, and an alumina boat containing iodine (ca. 5 g) was placed upstream, approximately 1 cm outside of the heated zone of the furnace. Multiple substrates prepared according to the methods above were placed at various locations downstream to allow multiple substrate temperatures to be examined during a single reaction. Argon (99.999% pure) was flowed at atmospheric pressure through the reaction tube at a high rate (100 sccm) before synthesis and during the temperature ramping to flush the quartz tube, and then reduced to the lower flow rate of 7 sccm during the NW synthesis. The reactions were kept at a temperature of 900 °C (*T*1 at the center of the furnace) for 2.5−3 h followed by a natural cool down. Thin dark gray deposition was clearly visible on the substrates and on the quartz tube wall near the substrates after the reaction. The reported temperatures were determined during the reactions using a thermocouple inserted into corresponding positions between the quartz tube and molded furnace insulation.

Structural Characterization. The morphology of the as-grown products was examined using a field emission scanning electron microscope (SEM, LEO SUPRA 1530). Samples used for powder X-ray diffraction analysis were prepared by scraping NWs off the growth substrate and spreading them onto a glass slide coated with vacuum grease. PXRD was collected on a Siemens STOE diffractometer using Cu Kα radiation. As-grown substrates were sonicated for 10 s at 30% power in a small amount of ethanol to disperse the NWs in solution. Samples for EDS analysis were prepared by repeatedly dispersing multiple aliquots of this sonicated NW solution onto a Ge substrate with a micropipette until the desired NW density had been obtained. TEM grids were prepared by

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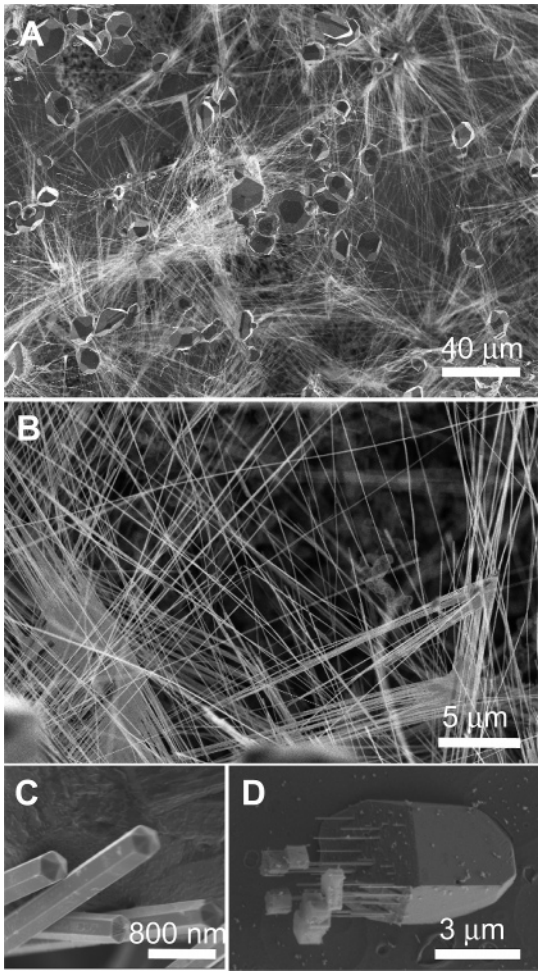

Figure 2. Representative SEM images of $CrSi_2$ nanowires found on substrates at various magnifications.

dispersing the NW/ethanol suspension solution onto lacey carbon TEM grids. The TEM analysis was carried out on a Philips CM200 TEM with an accelerating voltage of 200 kV.

Device Fabrication and Measurement. Two-terminal electrical devices were defined on nanowires randomly dispersed on degenerately doped Si substrates covered with a 600 nm thermal oxide layer using standard photolithography methods. The substrates were etched in buffered HF for 5 s before Ti/Au electrodes were deposited using e-beam metal evaporation. Room-temperature transport measurements were carried out on a probe station with a custom $I-V$ transport setup. Temperature-dependent transport studies were done on wire-bonded chips using a physical property measurement system (PPMS, Quantum Design) between 2 and 300 K.

Results and Discussion

Structural Characterization of the $CrSi_2$ Nanowires. SEM (panels A and B of Figure 2) reveals large quantities of straight and smooth NWs resulting from our CVT method with diameters ranging from 20 to 300 nm and lengths up to a few hundred micrometers (in some experiments). Experiments that followed the optimal conditions reported in the experimental section tended to produce longer NWs with smaller diameters ranging from 20 to 100 nm. As seen in Figure 2C, those NWs with large diameters also display hexagonal cross-sections and faceted sides. These NWs have clean and sharp faceted ends and do not show evidence of

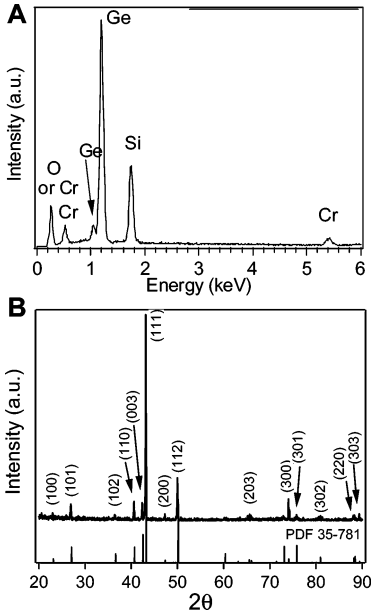

Figure 3. (A) EDS and (B) powder X-ray diffraction pattern of $CrSi_2$ nanowires.

catalyst particles. Notably, no catalytic caps of any type were ever observed in any of the samples examined. As evident from Figure 2A, most of the as-grown samples also contain micrometer-sized crystals together with NWs. Interestingly, NWs occasionally appear to grow epitaxially "out" from such crystals in parallel and additional microcrystals can also grow on the tips of the NWs (Figure 2D).

Quantitative energy dispersive spectroscopy (EDS) analysis (Figure 3A) revealed the composition of the NWs to be 36% chromium and 64% silicon, confirming the 1:2 Cr:Si composition of the NWs within the error of the methods. The Ge peaks come from the Ge substrates employed. Powder X-ray diffraction (PXRD), as shown in Figure 3B, confirmed the NWs to be the hexagonal $CrSi_2$ phase. All diffraction peaks can be matched to those of $CrSi_2$ (space group $P6_222$, Pearson symbol $hP9$, structure type $CrSi_2$, $a = 4.4281$ Å and $c = 6.3691$ Å, $Z = 3$, JCPDS PDF35-781).[32] No other chromium silicide phases or other crystalline impurity phases are detectable by PXRD, which highlights the rational control of the Cr:Si phase afforded by our CVT methods.

Transmission electron microscopy (TEM) further confirms the structure and reveals the single-crystalline high-quality nature of the NWs. A low-magnification TEM image (Figure 4A) shows a representative $CrSi_2$ NW with a diameter of 65 nm. High-resolution TEM (HRTEM) image (Figure 4B) of a representative NW clearly shows lattice fringes of a single-crystal nanowire along the $[\bar{1}10]$ zone axis. The observed lattice spacings are measured to be 6.37, 2.11, and 2.23 Å, which correspond well to the (001) (6.368 Å), (111) (2.091 Å), and (110) (2.214 Å) lattice spacings of $CrSi_2$, respectively. The two-dimensional fast Fourier transform (FFT) (Figure 4B, inset) of the lattice-resolved image shows the reciprocal lattice peaks, which can be indexed to a hexagonal

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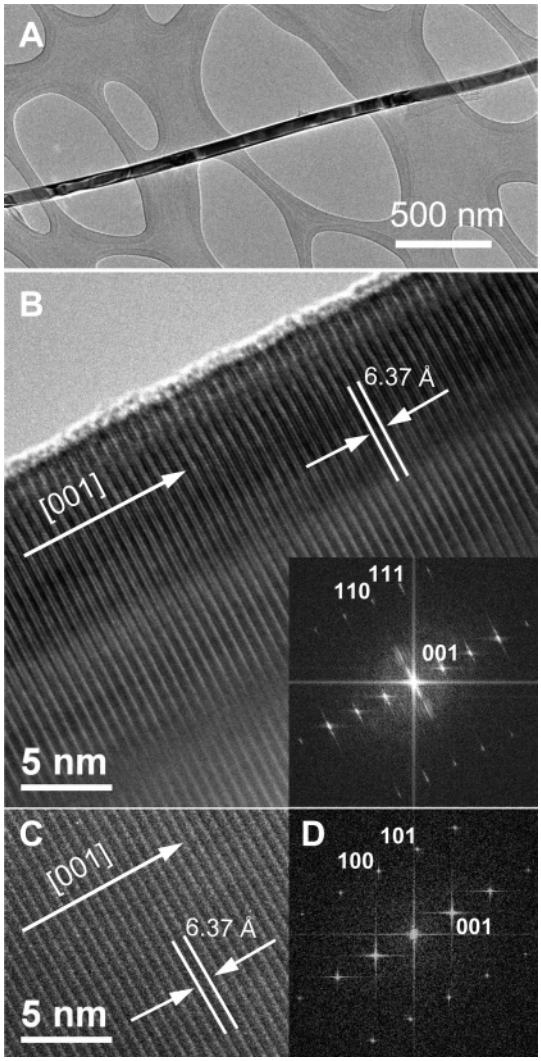

Figure 4. (A) Representative low-magnification TEM image of a $CrSi_2$ nanowire; (B) Representative HRTEM image of a $CrSi_2$ nanowire along the [$\bar{1}$10] zone axis and the corresponding two-dimensional FFT (inset); (C) HRTEM and (D) FFT of another nanowire along the [010] zone axis.

lattice with a lattice constant of $a = 4.43$ Å and $c = 6.37$ Å. Panels C and D of Figure 4 show the HRTEM and FFT of another NW along zone axis [010]. The ED patterns do not change as the electron beam is moved along the NW axes, indicating single-crystal structure. The indexed reciprocal lattices for all observed NWs show that the NW growth axis is parallel to the <001> direction, i.e., along the *c*-axis of the hexagonal structure, consistent with the observed facets (Figure 2C). All NWs are coated with a thin (1−2 nm) layer of amorphous silicon oxide, as expected for the surface oxidation of silicide in the air.[33]

Chemical Vapor Transport (CVT) Synthesis of Silicide Nanowires. In our typical CVT reactions in an atmospheric pressure flow reactor, about 5 g of the transport reagent iodine is sublimed and carried downstream, where it reacts with about 30 mg of $CrSi_2$ powder at high-temperature *T*1, which is usually kept at 900 °C for all reactions (eq 1). The resulting gas-phase chromium iodide and silicon iodide precursors are delivered to supply the chromium and silicon for NW growth at lower-temperature *T*2 downstream. Deposition of micrometer-sized crystals and NWs (when other conditions are appropriate, vide infra) was observed on substrates in the temperature (*T*2) range from 700 to 875 °C. Within this temperature range, the NW-to-crystal ratio increased with decreasing temperature, whereas the total $CrSi_2$ deposition amount (on the basis of optical micrograph estimates) increased with increasing temperature. Notably, if the transport reagent iodine was not used in the reactions under otherwise identical conditions, no deposition is observed on the substrates, highlighting the critical role CVT plays in the delivery of source silicide materials. Lower Ar flow rates were found to favor more effective silicide delivery and better NW growth, as easily checked by the amount of silicide weight loss from the source boat. An argon flow rate of 7 sccm was determined to be the optimal flow rate. Only one crystalline phase of $CrSi_2$ was ever observed for either crystals or NWs on the growth substrates on the basis of PXRD, highlighting the phase control afforded by the CVT method. Although some I_2 etching of the silicon substrates was observed, this does not appear to affect the phase of the deposited crystals and NWs. Electrical transport and thermoelectric measurements (vide infra) show that holes are the majority carriers of these nanowires, which is inconsistent with silicon-rich $CrSi_2$. The etching is likely due to the fact that in the flow-reactor CVT we use, most of the sublimed iodine does not have the chance to react with the source material before being swept through the reactor by the carrier gas, unlike traditional sealed-tube CVT, in which a small amount of iodine is available to react repeatedly with the source material under equilibrium conditions. The large excess iodine could etch the silicon substrate when the thermodynamic conditions are conducive for forming SiI_4 (but not suitable for forming silicon from SiI_4) in the substrate temperature zone, but the SiI_4 formed is then swept downstream by the carrier gas and does not cause appreciable impact to the phase control of the nanowire formation.

It should also be emphasized that the flow through reactor design might not allow for equilibrium CVT reactions usually observed in conventional CVT single-crystal growth in sealed tubes.[29,30] In fact, the temperature profiles identified as the optimal conditions for efficient delivery of silicides (including crystals) and production of NWs in high yield are different from what was reported before.[30] Therefore, we believe that in the design of NW synthesis reactions using CVT method, the conventional CVT reaction conditions generally serve only as a starting point for experimental exploration.

To form NWs instead of crystals in high yield, it is necessary to use silicon substrates with a thin (1−2 nm) silicon oxide layer. An oxide thickness corresponding to 20 min in the "metal" etch solution (30% H_2O_2:37% HCl:H_2O = 1:1:5 v/v) at 70 °C or 60 min exposure to UV light was found to produce the thinnest NWs with highest deposition density. As shown in Figure 5A, using silicon substrates coated with thick (100 nm) thermal silicon oxide, large amounts of micrometer-sized $CrSi_2$ single crystals were produced even though the reactions are otherwise identical to those reported in the experimental section. Substrates with

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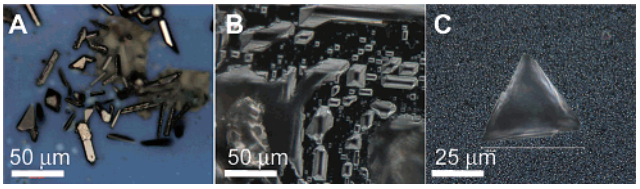

Figure 5. Dark-field optical micrographs of the growth substrates showing $CrSi_2$ crystals when (A) silicon substrates coated with 100 nm SiO_2, (B) freshly HF-etched Si(100), and (C) freshly HF-etched Si(111) substrates were attempted for nanowire growth under otherwise identical conditions.

no oxide layer or too thin an oxide layer also lead to crystal growth but no NWs (images B and C in Figure 5). Such critical oxide thickness dependence was also observed in the successful CVD growth of silicide NWs previously reported.[24,31] Although at the present we cannot fully explain the underlying mechanism, we believe they are universally related and are working on elucidating such general mechanistic details.

Slightly different from the previous CVD synthesis of silicide NWs, the presence of $Ni(NO_3)_2$ is also critical for producing large amounts of $CrSi_2$ NWs. $Ni(NO_3)_2$ was the only transition metal salt investigated that resulted in the growth of $CrSi_2$ NWs. Attempts at using solutions of $M(NO_3)_x$ (M = Cr, Fe, Al, Mn) with concentrations ranging from 0.002 to 0.2 M yielded only $CrSi_2$ crystals and no NWs. However, as noted earlier, no catalyst tips are visible on the faceted NW ends and trace amounts of Ni were never detected using EDS analysis. These strongly suggest that a vapor−liquid−solid (VLS) mechanism[20,27] commonly employed in NW growth is probably not responsible for these $CrSi_2$ NWs. The observation of NW growth from silicide crystals (Figure 2D) seems to suggest a vapor−solid[21] like mechanism, but this cannot explain the sensitive silicon oxide dependence discussed above. It is unknown what role the nickel salt plays in the NW growth process. It is possible that the trace amount of Ni from $Ni(NO_3)_2$ provides nucleation sites for vapor-phase-delivered precursors of Cr and Si in a 1:2 ratio. In fact, when the oxide thickness is not conducive for the formation of NWs (vide supra), the presence of nickel salt promotes the deposition of crystals in large quantities as well.

Because there are excellent heteroepitaxial lattice matches between the *c* face of the $CrSi_2$ hexagonal structure and the Si (111) surface,[34] we attempted to produce vertically aligned epitaxial $CrSi_2$ NWs on Si (111) substrates but with no success. It is possible that the thin silicon oxide layer prevents the epitaxial NW growth. Using freshly etched Si substrates yielded epitaxial $CrSi_2$ crystals on Si, as shown in Figure 5C.

Electrical Transport Properties of $CrSi_2$ Nanowires. Two-terminal electrical measurements were performed to determine the resistivity of the $CrSi_2$ NWs.[24,35] Figure 6A shows a representative current vs voltage ($I-V$) curve at room temperature showing linear behavior for these NWs. This suggests that an ohmic contact was formed for the NW

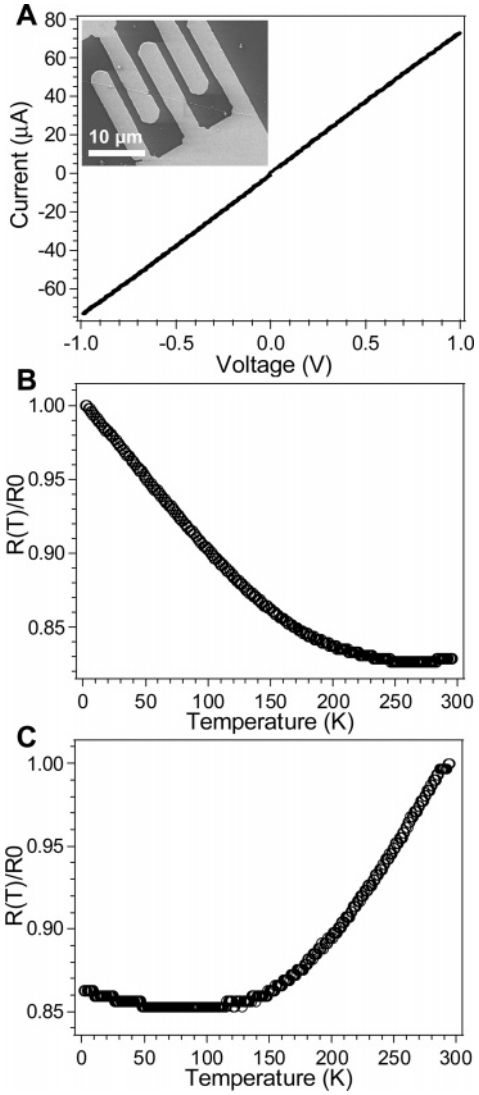

Figure 6. Electrical transport measurements on individual single-crystal $CrSi_2$ nanowires. (A) Room-temperature current vs voltage curves recorded for a two terminal device made of a $CrSi_2$ nanowire. (inset) SEM image of the device measured. (B, C) Temperature-dependent normalized two-terminal resistance of individual $CrSi_2$ nanowires displaying two types of behavior. The resistance, $R(T)$, is normalized by the maximum value $R0$ at 2 K for (B) and 300 K for (C).

devices, which is generally believed to be fairly easy because of the narrow band gap (0.35 eV) of the $CrSi_2$ semiconductor so long as the surface oxide is removed before making contact. Measurements were taken from multiple NW devices, and the NW lengths and diameters were estimated using SEM to calculate the average resistivity. The average resistivity of the $CrSi_2$ NWs was estimated to be 4.4×10^{-3} Ω cm, which is within the ranges of resistivities 1×10^{-3} to 1×10^{-2} Ω cm published previously for bulk $CrSi_2$ (including both single crystals and polycrystalline film).[1,9,12,36,37] The majority carrier in as-synthesized $CrSi_2$ is holes, on the basis of previous investigations.[1] The rather low resistivity (for a semiconductor) observed suggests that our as-grown $CrSi_2$ NWs are heavily doped. The actual resistivity of the $CrSi_2$ NWs may be even lower because of the likely contact

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resistance that cannot be accounted for by the simple two-terminal measurements.

Temperature-dependent transport measurements show two types of behaviors: for some NWs, the resistance increases monotonically with the decrease of temperature (Figure 6B), as expected for semiconductors. The total amplitude of the resistance change is not very significant over the fairly narrow temperature range allowed by the PPMS system, and a reliable fitting to extract the band gap was not possible. However, it was also sometimes observed that the resistance decreases with decreasing temperature (Figure 6C), which would be the typical behavior expected for the resistance of a metal. Such conflicting temperature dependence has been observed in single crystals of $CrSi_2$ before[36] and was attributed to the fact the temperature range from low T to room temperature is in the extrinsic region of the degenerate $CrSi_2$ semiconductor.[1,9] These conflicting temperature-dependence trends of resistivity can also be attributed to the varying levels of acceptor-doping concentration in NWs from different batches of synthesis (or even NWs from one batch of synthesis), underscoring the importance of precise control of doping during NW synthesis for further development and investigation of these important nanomaterials.

Conclusion

In conclusion, high-quality single-crystal $CrSi_2$ nanowires have been chemically synthesized for the first time using a chemical vapor transport (CVT) method and a likely non-VLS growth mechanism. Structural characterization confirms these NWs to be hexagonal $CrSi_2$, with NW growth in the <001> direction. Electrical transport measurements showed that the $CrSi_2$ NWs have an average resistivity of 4.4×10^{-3} Ω cm and behave like a degenerate semiconductor. These novel semiconducting silicide nanowire materials will be valuable as building blocks for silicon-compatible optoelectronic nanodevices in the IR range and for thermoelectric energy conversion. The thermoelectric properties of these NWs have been preliminarily evaluated and have recently been reported elsewhere.[38] Furthermore, we believe it is possible to use this CVT method to deliver stoichiometrically controlled precursors using corresponding source materials under suitable reaction conditions to synthesize NWs of other metal silicides, including other chromium silicide phases with different stoichiometries, so long as catalytic formation of nanowires can be enabled.

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